Abstract of the Disclosure

A resource including a plurality of elements, such as a cache memory having a plurality of addressable blocks or ways, is shared between two or more components based on the operation of an access controller. The access controller, controls which of the elements are accessed exclusively by a component and which are shared by two or more components. In one embodiment, the components include the execution of instructions in first and second threads in a multi-threaded processor environment. To prevent one thread from dominating the cache memory, a first mask value is provided for each thread. The access of the components to the cache memory is controlled by the first mask values. For example, the mask values can be selected so as to prevent a thread from accessing one or more of the ways in the cache (e.g., to evict, erase, delete, etc. a particular way in the cache). Also, the mask values can be set to allow certain of the ways in the cache to be shared between threads.

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